Claims

What is claimed is:

1. A random access memory circuit, comprising:

a plurality of memory cells;

at least one decoder coupled to the memory cells, the at least one decoder being configurable for receiving an input address and for accessing one or more of the memory cells in response thereto;

a plurality of sense amplifiers operatively coupled to the memory cells, the sense amplifiers being configurable for determining a logical state of one or more of the memory cells; and

a controller coupled to at least a portion of the sense amplifiers, the controller being configurable for selectively operating in at least one of a first mode and a second mode, wherein in the first mode the controller enables one of the sense amplifiers corresponding to the input address and disables the sense amplifiers not corresponding to the input address, and in the second mode the controller enables substantially all of the sense amplifiers.

2. The memory circuit of claim 1, wherein the controller dynamically changes the operating mode in response to at least one characteristic associated with the memory circuit.

3. The memory circuit of claim 2, wherein the at least one characteristic comprises at least one of a physical layout of the memory circuit, a clock frequency associated with the memory circuit, and a voltage supply associated with the memory circuit.

4. The memory circuit of claim 1, wherein the first mode comprises a power-saving mode and the second mode comprises a low-latency mode.

5. The memory circuit of claim 1, further comprising at least one multiplexer operatively coupled to at least a portion of the plurality of sense amplifiers, the multiplexer including at least one control input for receiving a select signal, the multiplexer connecting one

of the sense amplifiers coupled thereto to an output of the multiplexer in response to the select signal.

6. The memory circuit of claim 5, further comprising a latch circuit coupled to the output of the at least one multiplexer, the latch circuit at least temporarily storing an output of one of the sense amplifiers.

7. The memory circuit of claim 1, wherein the controller comprises a plurality of sense amplifier enable circuits, each of the sense amplifier enable circuits corresponding to a given one of the sense amplifiers, each of at least a portion of the plurality of sense amplifier enable circuits receiving a timing signal for selectively disabling the corresponding sense amplifier coupled thereto while the timing signal is inactive.

8. The memory circuit of claim 7, wherein the timing signal is a function of one or more characteristics associated with the memory cells.

9. The memory circuit of claim 7, wherein each of at least a portion of the sense amplifier enable circuits is configured such that the corresponding sense amplifier coupled thereto is disabled during a test mode of operation of the memory circuit.

10. The memory circuit of claim 1, wherein the controller is configurable for receiving a timing signal and a plurality of control signals, each of the control signals corresponding to a given one of the sense amplifiers, each of the sense amplifiers being selectively disabled in response to at least one of the timing signal and the corresponding control signal, the controller being operable in a third mode, wherein each of at least a portion of the control signals is initially set to enable the sense amplifier corresponding thereto during a time period in which a determination is performed as to whether the sense amplifier substantially corresponds to the input address, such that: (i) when the timing signal is set to enable the sense amplifiers before the determination is performed, the corresponding sense amplifier is enabled; and (ii) when the timing signal is set to enable the sense amplifiers after the determination is

performed, the corresponding sense amplifier is one of enabled and disabled, depending at least in part on whether or not, respectively, the input address substantially corresponds to the sense amplifier.

11. The memory circuit of claim 1, further comprising at least one test circuit configurable for operatively testing one or more components in the memory circuit during a test mode of operation of the memory circuit.

12. The memory circuit of claim 11, wherein the test circuit comprises a multiplexer, the multiplexer including a first input for receiving a test address and at least a second input for receiving a control signal used to selectively disable one or more of the sense amplifiers, the multiplexer being configurable for connecting the test address to an output of the multiplexer during a test mode of operation of the memory circuit.

13. The memory circuit of claim 1, further comprising:

at least one tag random access memory (RAM), the tag RAM including a plurality of memory cells and a plurality of data ways coupled to the memory cells in the tag RAM; and

a plurality of comparators, each of the comparators including a first input coupled to a corresponding one of the data ways, a second input for receiving at least a portion of the input address, and an output coupled to the controller, each of the comparators generating a control signal at its output that is representative of whether an address associated with a corresponding data way in the tag RAM substantially matches the input address.

14. A cache memory circuit, comprising:

a tag random access memory (RAM) including a plurality of memory cells and a plurality of data ways coupled to the memory cells for at least selectively reading a logical state of one or more of the memory cells;

a plurality of comparators, each of the comparators including a first input coupled to a corresponding one of the data ways, a second input for receiving at least a portion of an input address, and an output, each of the comparators generating a control signal at its output that is

representative of whether an address associated with a corresponding data way in the tag RAM substantially matches the input address; and

a data RAM circuit including:

a plurality of memory cells;

at least one decoder operatively coupled to the memory cells in the data RAM circuit, the at least one decoder being configurable for receiving the input address and for accessing one or more of the memory cells in response thereto;

a plurality of sense amplifiers operatively coupled to the memory cells in the data RAM circuit, the sense amplifiers being configurable for determining a logical state of one or more of the memory cells; and

a controller coupled to at least a portion of the sense amplifiers, the controller being configurable for selectively adapting a latency of the cache memory circuit.

15. The cache memory circuit of claim 14, wherein the controller is configured to selectively adapt the latency of the cache memory circuit by at least one of enabling and disabling the sense amplifiers based at least in part on a timing signal received by the controller and on a determination as to whether an address associated with a corresponding data way substantially matches the input address.

16. The cache memory circuit of claim 15, wherein the timing signal is a function of one or more characteristics associated with one or more memory cells in at least the data RAM.

17. The cache memory circuit of claim 14, wherein each of at least a portion of the comparators are configured to generate a control signal at its output that is at least initially set to enable a sense amplifier corresponding thereto during a period in which a determination is made as to whether an address associated with the corresponding data way substantially matches the input address.

18. The cache memory circuit of claim 14, wherein the controller is configurable for receiving a timing signal and the plurality of control signals from the comparators, each of the

control signals corresponding to a given one of the sense amplifiers, each of the sense amplifiers being selectively disabled in response to at least one of the timing signal and the corresponding control signal, each of at least a portion of the control signals being initially set to enable the sense amplifier corresponding thereto during a time period in which a determination is performed as to whether the sense amplifier associated with a given one of the data ways substantially corresponds to the input address, such that: (i) when the timing signal is generated before the determination is performed, the corresponding sense amplifier is enabled; and (ii) when the timing signal is generated after the determination is performed, the corresponding sense amplifier is one of enabled and disabled, depending at least in part on whether or not, respectively, the input address substantially corresponds to the data way associated with the sense amplifier.

19. The cache memory circuit of claim 14, wherein the controller dynamically changes the latency of the cache memory circuit in response to at least one characteristic associated with the cache memory circuit.

20. The cache memory circuit of claim 14, further comprising at least one multiplexer operatively coupled to at least a portion of the plurality of sense amplifiers, the multiplexer including at least one control input for receiving a select signal, the multiplexer connecting one of the sense amplifiers coupled thereto to an output of the multiplexer in response to the select signal.

21. The cache memory circuit of claim 14, further comprising at least one test circuit configurable for operatively testing one or more components in the cache memory circuit during a test mode of operation of the memory circuit.

22. A semiconductor device comprising at least one random access memory circuit, the random access memory circuit comprising:

a plurality of memory cells;

at least one decoder coupled to the memory cells, the at least one decoder being configurable for receiving an input address and for accessing one or more of the memory cells in response thereto;

a plurality of sense amplifiers operatively coupled to the memory cells, the sense amplifiers being configurable for determining a logical state of one or more of the memory cells; and

a controller coupled to at least a portion of the sense amplifiers, the controller being configurable for selectively operating in at least one of a first mode and a second mode, wherein in the first mode the controller enables one of the sense amplifiers corresponding to the input address and disables the sense amplifiers not corresponding to the input address, and in the second mode the controller enables substantially all of the sense amplifiers.